CH7101A HDMI to VGA Converter

FEATURES

- HDMI Receiver compliant with HDMI 1.4 specification
- Analog RGB output for VGA with Triple 9-bit DAC up to 200 MHz pixel rate. Sync signals can be provided in separated or composite manner. Support VESA and CEA timing standards up to WUXGA 1920x1200@60Hz and 1920x1080@60Hz
- On-chip Audio encoder which support 2 channel IIS/ S/PDIF audio output
- VGA output is compliant with VESA VSIS v1r2 specification
- MCU embedded to handle the control logic
- Support device boot up by automatically loading firmware from on-chip flash Boot ROM
- Integrated EDID Buffer
- Crystal Free architecture
- VGA connection detection supported
- HDMI input detection supported
- Support Auto Power Saving mode and low stand-by current
- Support YCC to RGB conversion in ITU-R BT.601 and 709 color space
- IIC slave interface and HDMI DDC interface are available for debug and firmware update.
- Low power architecture
- RoHS compliant and Halogen free package
- Offered in 40-Pin QFN package (5 x 5 mm)

APPLICATION

- Notbook/Ultrabook
- Tablet Device
- Handheld/Portable Device
- Digital Video Systems
- HDMI to VGA Adapter/Docking Station
- Car Entertainment Device

GENERAL DESCRIPTION

Chrontel's CH7101A is a low-cost, low-power semiconductor device that consists of HDMI receiver, three separate 9-bit video Digital-to-Analog Converters (DACs) and audio encoder, which can convert HDMI signals into VGA outputs at a maximum conversion rate of 200MHz with IIS or SPDIF audio output.

The HDMI Receiver integrated is compliant with HDMI 1.4b. The DACs are based on current source architecture. And the VGA output meet VESA VSIS v1r2 clock jitter target. With sophisticated MCU and the Boot ROM embedded, CH7101A support auto-boot and EDID buffer. Take the advantage of Firmware auto loaded from the embedded Boot ROM, CH7101A can support HDMI input detection, DAC connection detection and determine to enter into Power saving mode automatically.

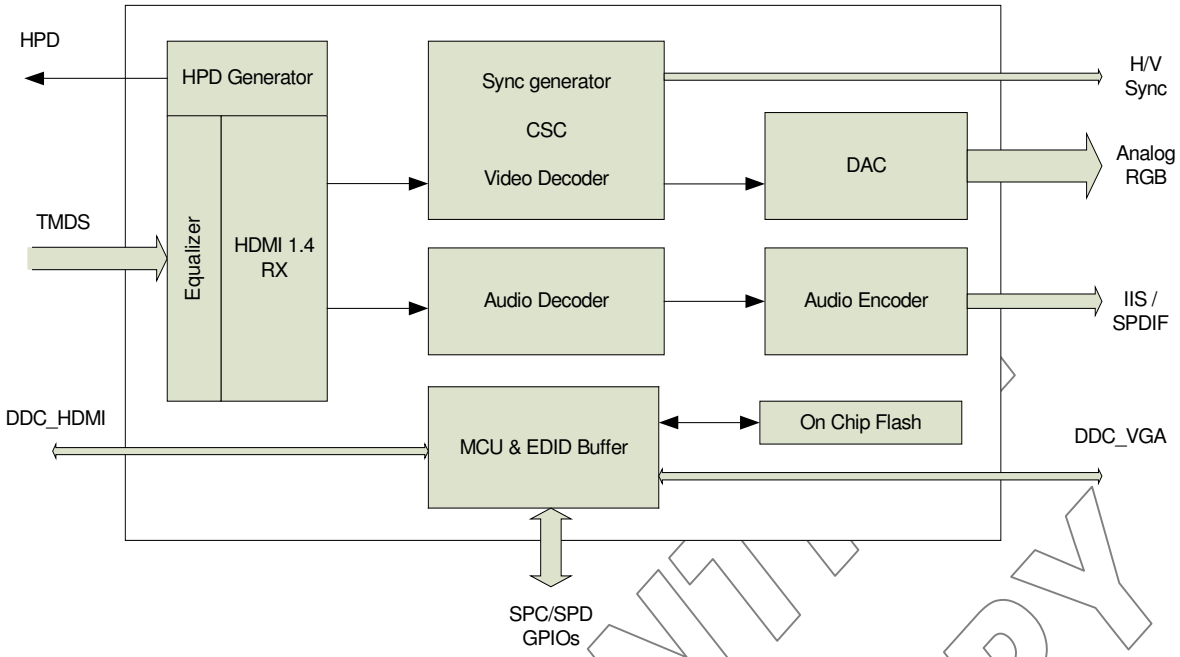

Figure 1: CH7101A Functional Block Diagram

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1.0 PIN-OUT

1.1 Package Diagram

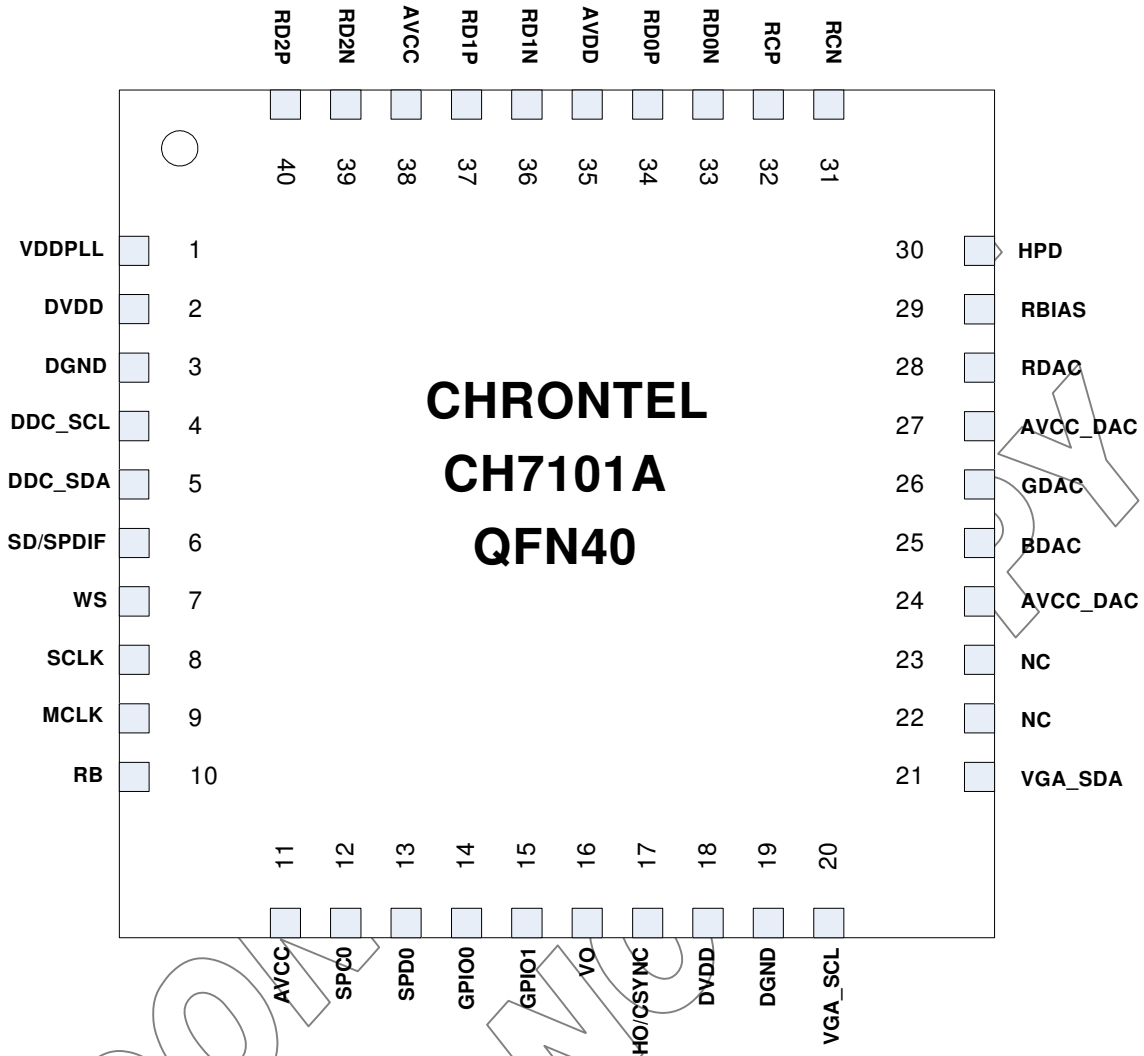

Figure 2: CH7101A 40-pin QFN pin out

1.2 Pin Description

Table 1: Pin Name Descriptions

Pin #	Type	Symbol	Description
4	In	DDC_SCL	**Serial Port Clock to HDMI/DVI Transmitter** This pin functions as the clock bus of the serial port to HDMI or DVI DDC transmitter. This pin requires a pull-up 47 kΩ resistor to the desired voltage level
5	In/out	DDC_SDA	**Serial Port Data to HDMI/DVI Transmitter** This pin functions as the data bus of the serial port to HDMI or DVI DDC transmitter. This pin requires a pull-up 47 kΩ resistor to the desired voltage level
6	Out	SD/SPDIF	**I2S Serial Data or SPDIF Output**
7	Out	WS	**I2S Word Select**
8	Out	SCLK	**I2S Continuous Serial Clock**
9	Out	MCLK	**I2S System Clock**
10	In	RB	**Chip Reset** Low to 0V for reset. Typical High level is 3.3V
12	In	SPC0	**Serial Port Clock Input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required
13	In/out	SPD0	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required
14,15	In/Out	GPIO	**General Purpose Input/Output**
16	Out	VO	**Vertical Sync Signal Output** The amplitude of this pin is from 0 to AVCC
17	Out	HO/CSYNC	**Horizontal Sync Signal Output** The amplitude of this pin is from 0 to AVCC It also functions as a Composite sync output
20	Out	VGA_SCL	**Serial Port Clock Output to VGA Receiver** The pin should be connected to clock signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level
21	In/Out	VGA_SDA	**Serial Port Data to VGA Receiver** The pin should be connected to data signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level
22,23	NC	NC	**Not Connected**
25	Out	BDAC	**VGA Blue Component DAC output**
26	Out	GDAC	**VGA Green Component DAC output**
28	Out	RDAC	**VGA Red Component DAC output**
29	In	RBIAS	**Current Set Resistor Input** This pin sets the DAC current. A 10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces
30	Out	HPD	**HDMI Receiver Hot Plug output**
31,32,33, 34,36,37, 39,40	In	RD[2:0]P/N RCP/N	**HDMI TMDS Input** HDMI differential clock and data input pairs
1	Power	VDDPLL	**PLL Power Supply (1.2V)**
2,18	Power	DVDD	**Digital IO Power Supply (1.2V)**

3,19	Power	DGND	**Digital Ground**
11, 38	Power	AVCC	**Analog Power Supply (3.3V)**
24,27	Power	AVCC_DAC	**Analog DAC Power Supply (3.3V)**
35	Power	AVDD	**HDMI Receiver Analog Power Supply (1.2V)**
Pad	Power	GND	**Power Supply Ground**

2.0 FUNCTIONAL DESCRIPTION

2.1 HDMI Receiver

CH7101 HDMI Receiver is compliant with HDMI specification 1.4 and DVI specification 1.0. It supports VESA and CEA timing standards up to UXGA and 1920x1080@60Hz.

CH7101 HDMI receiver supports input video timing detection.

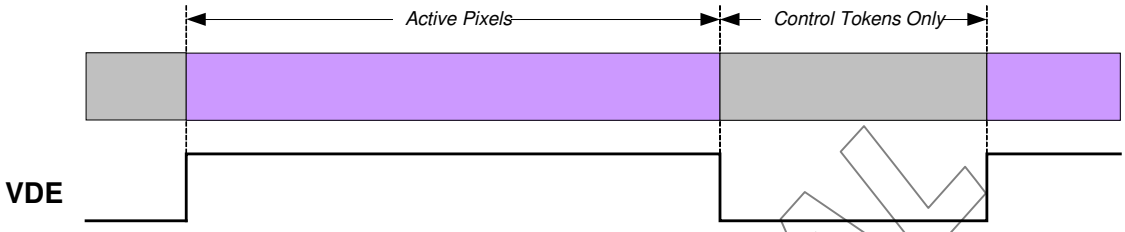

Figure 3: DVI Mode decoder

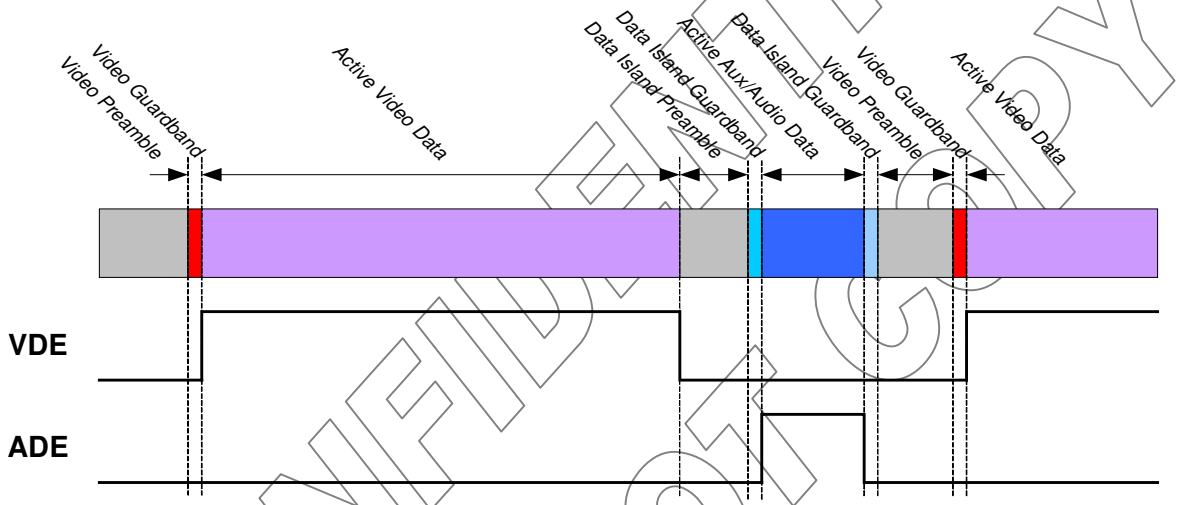

Figure 4: HDMI Mode decoder

CH7101's audio block supports 2 channel audio stream receiving. High performance audio recovery with low jitter is achieved by the internal advanced audio clock re-generation block.

An internal 2 blocks EDID is embedded which can be programmed by CH7101 Host or embedded MCU upon power ON. The EDID can be used as 1 or 2-block EDID.

2.2 VGA Encoder

The CH7101 can support analog RGB output up to 1080P through triple video DACs, and the DAC supports pixel rate up to 200MHz. The de-serialized data from the HDMI Receiver, after proper decoding and image enhancement process, are transported to the video DACs. This operating mode uses 8-bits of the DAC's 9-bit range, and provides a nominal signal swing of 0.7V(depending on DAC Gain setting in control registers) when driving a 75Ω doubly terminated load. No scaling, scan conversion or flicker filtering is applied.

2.2.1 Sync Mode

Vertical sync and horizontal sync signal, after proper decoding, are buffered internally, and can be output to drive the VGA monitor. Composite sync output is also supported. The type of composite sync can be programmed through register map.

Table 2: Composite sync type

CSSEL[2:0]	Composite sync type
0	Vsync XOR Hsync
1	Vsync OR Hsync
2	Vsync AND Hsync

2.2.2 DAC Single/Double Termination

The DAC output of the chip can be single terminated or double terminated. Using single termination will save power consumption while double termination is likely to minimize the effect of the cable. Single or double termination is controlled by register SEL_R.

2.2.3 DAC Connection Detection

The chip can detect the VGA monitor connection by DAC sense. It can detect which DAC are connected, short to ground or not connected.

2.3 Audio Encoder and Output

The 2 channel audio data recovered from HDMI data package can be encoded and output in format of IIS or SPDIF.

For I2S output, CH7101 supports the following formats:

- left-justified I2S mode, 16bits/20bits/24bit
- right-justified I2S mode, 16bits/20bits/24bit
- standard I2S mode, 16bits/20bits/24bit

For SPDIF output, CH7101 supports audio sample frequencies from 32Khz to 192kHz.

3.0 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	All 1.2V power supplies relative to GND All 3.3V power supplies relative to GND	-0.5 -0.5		1.5 5.0	V
	Input voltage of all digital pins	GND – 0.5		AVCC+0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature (Commercial / Automotive Grade 4)	0		70	°C
T_{AMB}	Ambient operating temperature (Industrial / Automotive Grade 3)	-40		85	°C
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS1}	Vapor phase soldering (5 seconds)			260	°C
T_{VPS2}	Vapor phase soldering (11 seconds)			245	°C
T_{VPS3}	Vapor phase soldering (60 seconds)			225	°C

Note:
1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce permanent damage.
3. The digital input voltage will follow the I/O supply voltage (AVCC).

3.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
DVDD	Digital Power Supply	1.08	1.2	1.32	V
DGND	Digital ground		0		V
AVDD	Analog HDMI receiver power supply	1.08	1.2	1.32	V
VDDPLL	Analog PLL power supply	1.08	1.2	1.32	V
AVCC	Analog 3.3V power supply	2.97	3.3	3.63	V
AVCC_DAC	Analog DAC power supply	2.5	3.3	3.63	V
AVSS	Analog ground		0		V
VDD12	All 1.2V power supply(including DVDD, VDDPLL, AVDD)	1.08	1.2	1.32	V
VDD33	All 3.3V power supply(including AVCC, AVCC_DAC)	2.5	3.3	3.63	V

3.3 Electrical Characteristics

(Test Conditions: T_A = 0°C – 85°C, VDD12=1.2V± 5%, VDD33 =2.5V – 3.5V)

Symbol	Description	Min	Typ	Max	Units
	Video DAC Resolution		9		bits
	Full scale output current of each DAC		24		mA

	INL		± 0.8		LSB
	DNL		± 0.5		LSB
I_{VDD12}	Total current for 1.2V power supply (1080P, 148.5MHz Mode)		96		mA
	Total current for 1.2V power supply (1600x1200, 162MHz Mode)		98		mA
	Total current for 1.2V power supply (1920x1200, 193.25MHz mode)		106		mA
I_{VDD33}	Total current for 3.3V power supply (1080P, 148.5MHz Mode)		120		mA
	Total current for 3.3V power supply (1600x1200, 162MHz Mode)		122		mA
	Total current for 3.3V power supply (1920x1200, 193.25MHz mode)		123		mA
I_{PD}	Total Power Down Current		120		uA

Note:
While the AVCC_DAC is 2.5V, total Power Consumption can be decreased to about 443mW in 1080P mode.

3.4 Digital Inputs / Outputs DC Specifications

(Test Conditions: T_A = 0°C – 85°C, VDD12=1.2V± 5%, VDD33 =2.5V – 3.5V)

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	serial port data (SPD/SPC) Output Low Voltage	IOL = 3.0 mA	GND-0.5		0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		2.0		AVCC + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.7	V
V_{HYS}	Hysteresis of Serial Port Input		0.25			V
V_{DDCOL}	DDC serial port (DDC_SCL, DDC_SDA) output Low voltage		GND-0.5		0.4	
V_{DDCIH}	DDC serial port (DDC_SDA) input high voltage		2.0		V_{DDC} (2)+ 0.3V	V
V_{DDCIL}	DDC serial port (DDC_SDA) input Low voltage		GND-0.5		0.7	V
V_{DATAH}	Data Output (1) High Voltage		2.0		AVCC + 0.5	V
V_{DATAL}	Data Output(1) Low Voltage		GND-0.5		0.4	V

Notes:
1. Applies to HO, VO.
2. Applies to DDC_SCL, DDC_SDA,HPD, V_{DDC} is DDC Standard voltage.

3.5 HDMI Receiver AC Specifications

Symbol	Description	Min	Typ	Max	Unit
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew			0.4	T_{bit}
T_{CCS}	Channel to Channel Differential Input Skew			10	T_{bit}
T_{IJIT}	Differential Input Clock Jitter Tolerance			0.3	T_{bit}
F_{RXC}	TMDS CLK Frequency (HDMI mode)	25		200	MHz

3.6 I2S Audio AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
T_{sck_d}	SCLK Clock Duty Cycle	CL = 10pF	40%		60%	Tsck
T_{sck_h}	SCLK Clock High Time	CL = 10pF	40%		60%	Tsck
T_{sck_l}	SCLK Clock LOW Time	CL = 10pF	40%		60%	Tsck
T_s	Setup Time of SCLK	CL = 10pF	40%			Tsck
T_h	Hold Time of SCLK	CL = 10pF	40%			Tsck

Notes:
Tsck is SCLK Clock Period

3.7 SPDIF Audio AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
T_{spdif_d}	SPDIF Duty Cycle	CL = 10pF	90%			UI

4.0 PACKAGE DIMENSION

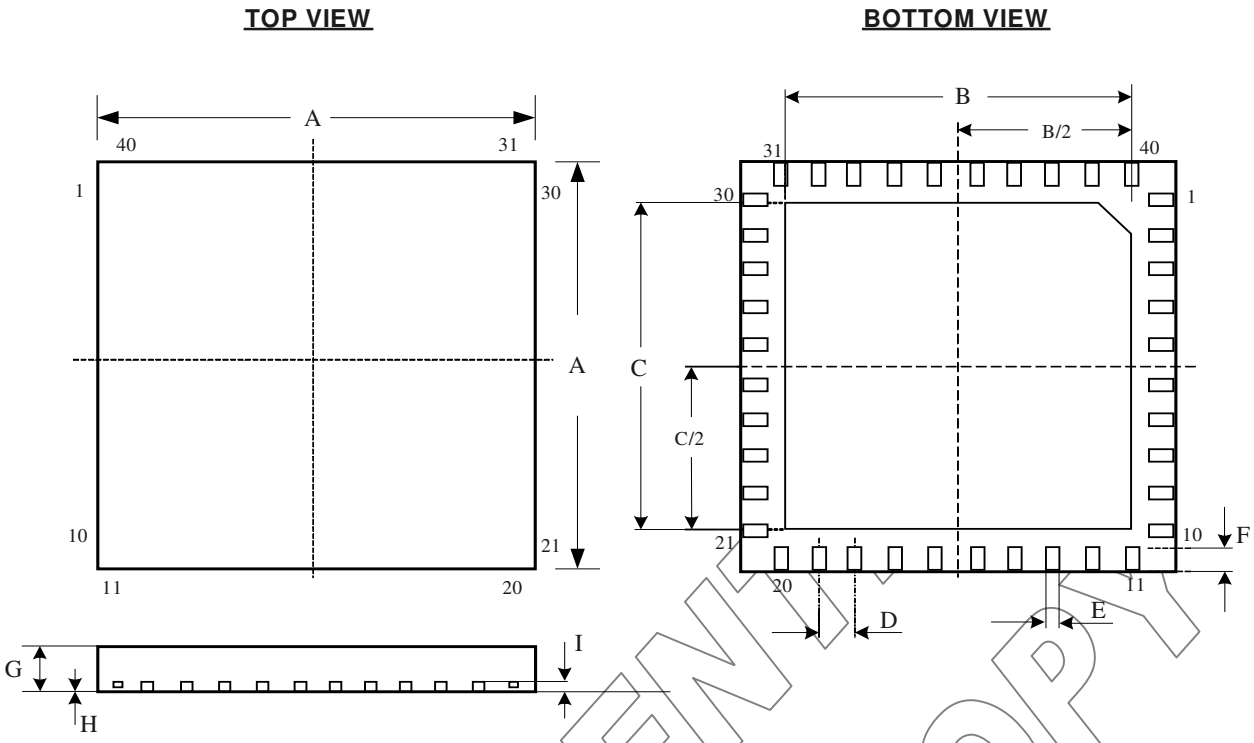

Figure 5: 40 Pin QFN Package

Table 3: Table of Dimensions

No. of Leads		SYMBOL								
40 (5 X 5 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	4.90	3.20	3.20	0.4	0.15	0.35	0.7	0	0.20
	MAX	5.10	3.75	3.75		0.25	0.55	0.8	0.05	0.203

Notes:
Conforms to JEDEC standard JESD-30 MO-220.

5.0 Revision History

Rev. #	Date	Section	Description
0.1	09/13/2012	All	First release.
0.2	09/27/2012	Figure 1 3.3	Modified the Block Diagram Update the power consumption
0.3	10/10/2012	3.1 3.3	Update the absolute maximum ratings Update the power consumption
0.4	10/16/2012	2.2.4	Delete the image process description
0.5	10/19/2012	Feature 3.3	Update the Feature Update the Power Consumption
0.6	11/23/2012	Feature 2.4	Update the Feature Delete 2.4

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ORDERING INFORMATION

Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity
CH7101A-BF	40 QFN, Lead-free	Commercial : 0 to 70°C	490/Tray
CH7101A-BFI	40 QFN, Lead-free	Industrial : -40 to 85°C	490/Tray

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